Effects of Gate Length on the Performance of a Top Gate Silicon Nanowire on Insulator (SOI) Transistor

Sishir Bhowmick, Redwan Noor Sajjad and Quazi D. M. Khosru

***Abstract*—The effects of gate length L_g on the performance of a top gate silicon nanowire on insulator transistor are studied using three dimensional quantum simulation. From the study it is found that the inverse subthreshold slope and on/off current ratio are very sensitive to gate length. Significant improvement in subthreshold slope and on/off current ratio can be achieved using relatively longer gate with thin gate oxide. This improvement in the subthreshold region is due to better control of channel potential with longer gate. As a result of that the tunneling current through the conduction band is significantly suppressed in the subthreshold regime and there is an improvement in the subthreshold slope and on/off current ratio. Performance metrics such as transconductance g_m, intrinsic switching delay τ_S and unity current gain frequency f_T of the device are also calculated and it is found that the on state performance of the device degrades with longer gate as all three parameters degrade with increased gate length.**

***Index Terms*—Silicon Nanowires (SiNWs), subthreshold slope, on state performance.**

I. Introduction

Scaling the transistor sizes has made significant improvement in the cost effectiveness and performance of integrated circuit over the last few decades. The bulk CMOS technology is rapidly approaching the scaling limit and hence alternate materials or device structures are essential for future electronic devices. One dimensional nanostructures such as the carbon nanotubes and silicon nanowires are the attractive materials for future nanoelectronics because their electronic properties can be controlled in a very predictable and effective manner. Controlled growth of silicon nanowires (SiNWs) down to 3 nm diameter [1], their applications as field-effect transistors (FETs) [2]–[5], logic gates [6], and sensors [7] have been demonstrated.

In this paper, we study the effects of gate length L_g on the performance of a top gate silicon nanowire on insulator trasistor. The gate length L_g has a very significant effect on the performance of the device in the sub-threshold region as well as on the performance metrics. The improvement in the subthreshold region is mainly due to the suppression of tunneling current in the off state as the tunnel barrier control improves with longer gate [8], [9]. The gate capacitance of the device increases and the transconductance degrades with increased gate length which result in increased intrinsic switching delay and reduced unity current gain frequency with longer gate.

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II. Simulation Model

In this study, the three dimensional (3D) Poisson's equation has been solved self consistently with effective mass Schrodinger's equation. The 3D Poisson's equation in cartesian coordinates is

$$\frac{\partial}{\partial x}\left(\epsilon\frac{\partial V}{\partial x}\right)+\frac{\partial}{\partial y}\left(\epsilon\frac{\partial V}{\partial y}\right)+\frac{\partial}{\partial z}\left(\epsilon\frac{\partial V}{\partial z}\right)=-\frac{\rho}{\epsilon_o}, \quad (1)$$

where ϵ_o is the free space permittivity, ϵ is the relative dielectric constant, V is the 3D potential, and ρ is the charge density, which is non-zero in silicon nanowire only. Poisson kernel is created by discretizing Eq. (1) using finite difference method. Potential is fixed at the gate metal and zero field boundary condition is applied at the source and drain ends and at the exposed surfaces of dielectric. There the normal component of electric field is set to zero. Standard Newton Raphson method is used to solve Poisson's equation.

The Schrodinger's equation in 3D cartesian coordinates is

$$-\frac{\hbar^2}{2}\left[\frac{\partial}{\partial x}\left(\frac{1}{m_x}\frac{\partial\psi}{\partial x}\right)+\frac{\partial}{\partial y}\left(\frac{1}{m_y}\frac{\partial\psi}{\partial y}\right)+\frac{\partial}{\partial z}\left(\frac{1}{m_z}\frac{\partial\psi}{\partial z}\right)\right]=E\psi \quad (2)$$

where ψ is the wave function, m_x, m_y, and m_z are the effective masses in device coordinates, and $\hbar$ is the reduced Plank's constant. The nanowire is grown in $\langle 100\rangle$ direction, which is device x coordinate in our study. Ballistic transport is assumed. Recursive Green's function algorithm (RGFA) [10] is used to solve Schrodinger's equation for charge density and current calculations. The open boundary condition in transport direction (x) is included in Schrodinger's equation via self-energy matrices. Hard-wall boundary condition is used in the transverse directions (y and z). For RGFA, the layer (cross-section) Hamiltonian and layer-to-layer coupling matrices are created by discretizing Eq. (2) using finite difference method. The charge density at each grid point of the Lth layer (cross-section) is calculated from

$$\rho_i=(4e)\int\frac{dE}{2\pi}\mathrm{diag}\left\{f_S A^L_{i,i}+f_D\left[A_{i,i}-A^L_{i,i}\right]\right\}, \quad (3)$$

where e is the electronic charge, f_S and f_D are the source and drain Fermi functions, respectively, and the factor 4 includes spin plus valley degeneracy. The charge density is calculated for each pair of valley and summed over the pairs to obtain the total charge density. The full spectral function is calculated from the imaginary part of retarded Green's function $A_{i,i}=-2\mathrm{Im}\left(G_{i,i}\right)$, where $G=(E-H-\Sigma)^{-1}$. The left spectral function is calculated from $A^L_{i,i}=G_{i,1}\Gamma_{1,1}G^\dagger_{i,1}$, where $\Gamma_{1,1}=i\left(\Sigma_S-\Sigma_S^\dagger\right)$ is the broadening function and the self-energy

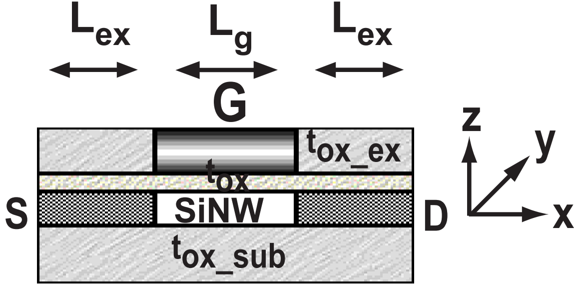

Fig. 1. Device cross section used for simulation. The device coordinates are also shown.

is calculated from $\Sigma_S = t_{1,0} g_{0,0} t_{0,1}$. Here $t_{0,1}$ is the coupling matrix between the 0th and 1st layers (cross-sections) and $g_{0,0}$ is the surface Green's function calculated using decimation method [11].

The self-consistent loop starts with an initial guess of the potential profile. Anderson mixing [12] scheme is used to accelerate convergence. Once the convergence is achieved, the coherent drain current is calculated from

$$I_D = \frac{2e}{h} \int dE \; T(E) \left(f_S - f_D \right), \tag{4}$$

where transmission $T(E)$ is calculated from [10]

$$T(E) = \mathrm{tr} \left(\Gamma_{1,1} \left[A_{1,1} - G_{1,1} \Gamma_{1,1} G^{\dagger}_{1,1} \right] \right). \tag{5}$$

III. Simulation Results

The top gate silicon nanowire on insulator device used in our simulation is shown in Fig. 1. The silicon nanowire is placed on a thick substrate oxide layer t_{ox-sub}. The gate oxide of thickness t_{ox} is grown on the nanowire. An ultra-thin gate metal is deposited on the top of the gate oxide and the exposed regions on both sides of the gate metal are covered by oxide t_{ox-ex}. The nanowire has a square cross section of 5×5 nm^2 with a band gap E_g of 1.38 eV (calculated from the E-K relation). The doped source-drain extension L_{ex} is of the length of 20 nm and fully ionized uniform donor concentration of 1.65 $\times 10^{19}$ cm^{-3} is assumed. The channel is intrinsic. The substrate oxide, the extended oxide and also the gate oxide are assumed to be SiO_2 with a dielectric constant of 3.9. The gate metal is assumed to have the same work function as that of nanowire. The gate oxide thickness t_{ox} is considered to be 1 nm for this simulation. The t_{ox-sub} value of 5 nm and the t_{ox-ex} value of 5 nm are considered for Poisson solver so that the fringing electric fields emanating from the gate metals are calculated correctly. Our simulation is modeled using bulk effective mass approximation whose accuracy for wire cross section of 5×5 nm^2 and above has been varified [13], [14].

The simulated off current versus gate length and on current versus gate length are shown in Fig.2. The off and on currents are the drain currents corresponding to V_{GS} = 0 V, V_{DD} = 0.5 V and V_{GS} = 0.7 V, V_{DD} = 0.5 V respectively. From the figure we see that the on state currents for different gate lengths are of the same order but the off currents significantly reduce with increased gate length. For the change in gate length from 5 nm to 10 nm, on current reduces from 19.2 μA to 11.3 μA while the off current reduces from 0.047 μA to 1.23×10^{-5} μA. The scaling behavior of inverse subthreshold slope and on/off current ratio with gate length L_g are shown in Fig. 3. Change in gate length from 5 nm to 10 nm improves the on/off current ratio by three orders of magnitude and the inverse subthreshold slope from 141.68 mV/dec to 82.59 mV/dec. Device performance degrades with shorter gate due to short

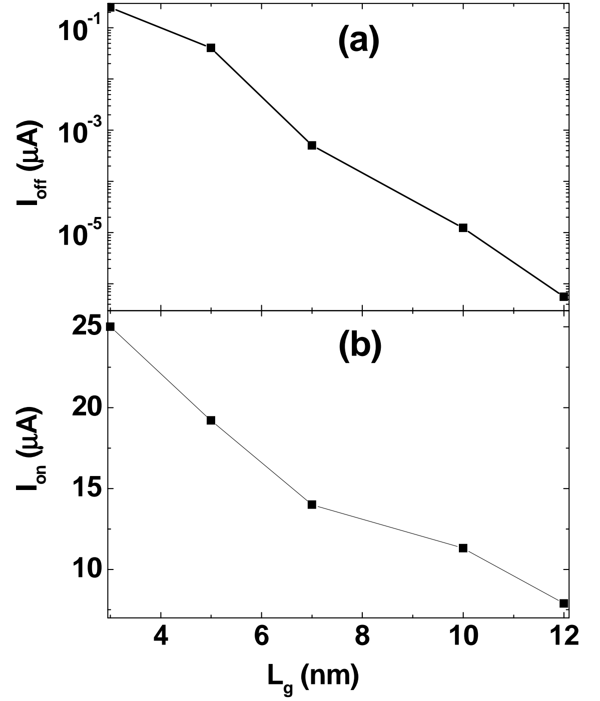

Fig. 2. (a) Off current versus gate length (b) On current versus gate length.

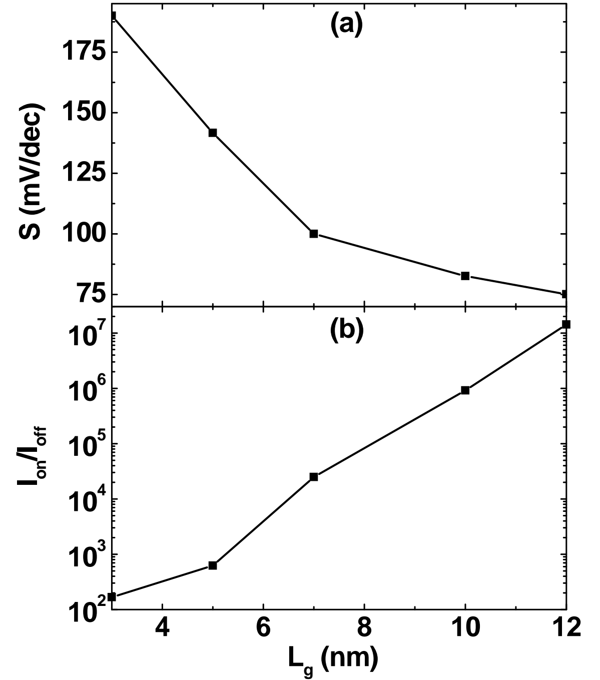

Fig. 3. (a) Inverse subthreshold slope versus gate length (b) on/off current ratio versus gate length.

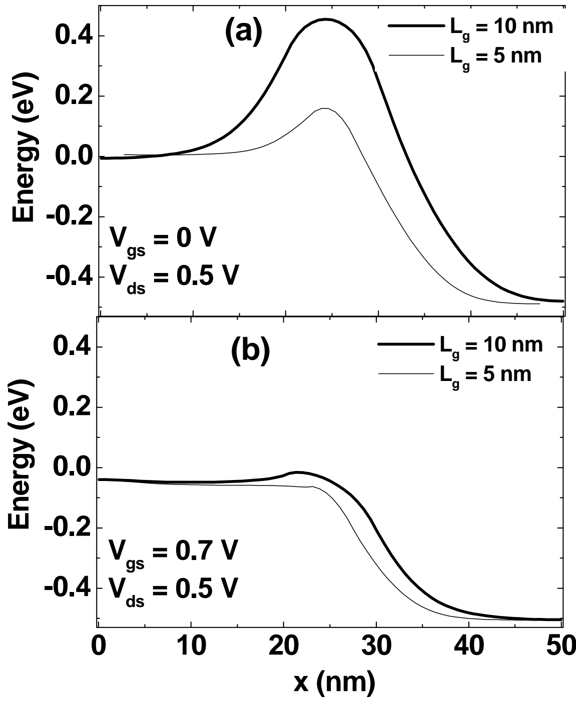

Fig. 4. (a) Conduction band profile in the off state (b) Conduction band profile in the on state.

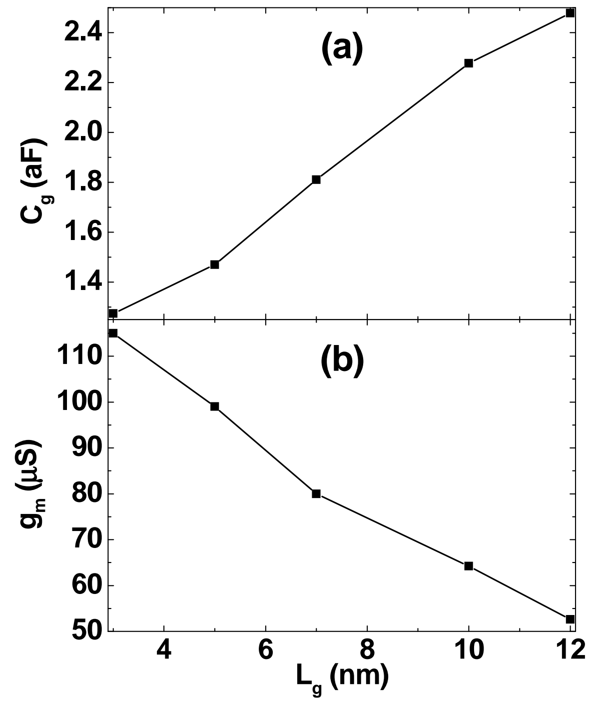

Fig. 5. (a) Gate capacitance versus gate length (b) Transconductance versus gate length.

channel effects. The physics behind this phenomenon can be understood from the conduction band profile shown in Fig.4. From the figure we see that in the off state the tunnel barrier height and width for L_g = 10 nm is significantly higher than that of L_g = 5 nm and therefore tunneling current (major component of off state current) for L_g = 10 nm through the barrier is greatly reduced compared to that of L_g = 5 nm while in the on state there is no significant the potential barrier difference for these two different gate length and hence the resulting on state currents are of the same order of magnitude.

Next we studied the performance metrics of the device with different gate lengths. For this study, the gate capacitance is calculated by integrating the fluxes emanating from the gate metal surfaces

$$C_g = \int\int dxdy \frac{\delta D_z}{\delta V_g} + \int\int dydz \frac{\delta D_x}{\delta V_g}, \quad (6)$$

where the first integral handles the electric fluxes emanating from the bottom surface of the gate metal and the second integral handles the fringing fields emanating from the two sides of the gate metal facing to the source and drain. The intrinsic switching delay is calculated from $\tau_S = C_g V_{DD}/I_{ON}$ and the intrinsic unity current gain frequency is from $f_T = g_m/2\pi C_g$. The on-state current I_{ON} is the drain current corresponding to V_{GS} = 0.7 V, V_{DD} is 0.5 V in our study, and the transconductance is calculated from $g_m = \partial I_D/\partial V_{GS}$.

The simulated gate capacitance versus gate length and transconductance versus gate length are shown in Fig. 5. From the figure we see that the gate capacitance increases and the transconductance decreases with increased gate length. As a result the intrinsic switching delay $\tau_S$increases and the unity current gain frequency f_T decreases with gate length. For the variation of gate length from 5 nm to 10 nm gate capacitance increases from 1.27 aF to 2.28 aF while the transconductance decreases from 99.3 μS to 64.2 μS. The intrinsic switching delay versus gate length and unity current gain frequency versus gate length are shown in Fig.6. From the figure wee see that both intrinsic switching delay and unity current gain

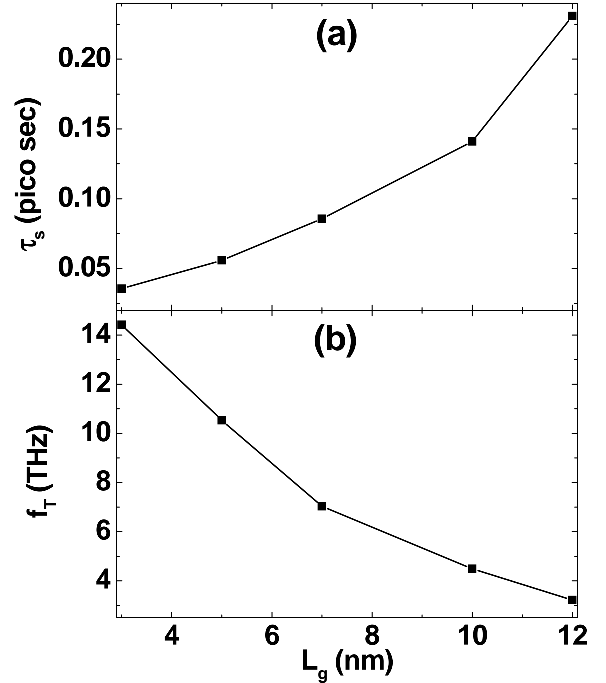

Fig. 6. (a) Intrinsic switching delay versus gate length (b) Unity current gain frequency versus gate length.

frequency degrades with longer gate length. For the variation of gate length from 5 nm to 10 nm intrinsic switching delay rises from 0.056 pico second to 0.23 pico second and unity current gain frequency decreases from 10.53 THz to 4.4879 THz.

IV. Conclusion

A three dimensional quantum simulation is performed to study the effects of gate length on the performance of a silicon nanowire on insulator transistor. The device performance in the subthreshold region namely on/off current ratio and inverse subthreshold slope improves with longer gate but the on state performance metrics namely transconductance, intrinsic switching delay and the unity current gain frequency degrades with increased gate length.

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