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The effects of doping, gate length, and gate dielectric on inverse subthreshold slope and on/off current ratio of a top gate silicon nanowire transistor

Sishir Bhowmick[1], Khairul Alam[2], and Quazi Deen Mohd Khosru[1]
Department of Electrical and Electronic Engineering
[1]Bangladesh University of Engineering and Technology, Dhaka-1000
[2]East West University, Dhaka-1212, Bangladesh
Email: sishir@eee.buet.ac.bd

***Abstract*— The effects of gate length L_g, gate dielectric constant ϵ_{ox}, gate oxide thickness t_{ox}, and sourc/drain doping concentration on inverse subthreshold slope and on/off current ratio of a top gate silicon nanowire on insulator device are studied using three dimensional quantum simulation. The variation of inverse subthreshold slope and on/off current ratio are very sensitive to gate length, gate dielectric constant, and oxide thickness and relatively less sensitive to doping concentration. Significant improvement in subthreshold slope and on/off current ratio can be achieved using high-K gate dielectric with thinner oxide and relatively longer gate. The key feature of this improvement is the better gate control of channel potential with longer L_g, higher ϵ_{ox}, and thinner t_{ox}. Due to better control of channel potential, the tunneling current through the conduction band is significantly suppressed in the subthreshold regime that improves the subthreshold slope and on/off current ratio.**

I. Introduction

Scaling the transistor sizes has made significant improvement in the cost effectiveness and performance of integrated circuit over the last few decades. The bulk CMOS technology is rapidly approaching the scaling limit and alternate materials or device structures are essential for future electronics. One dimensional nanostructures such as the carbon nanotubes and silicon nanowires are the attractive materials for future nanoelectronics because their electronic properties can be controlled in a predictable manner. Controlled growth of silicon nanowires (SiNWs) down to 3 nm diameter [1], their applications as field-effect transistors (FETs) [2]–[5], logic gates [6], and sensors [7] have been demonstrated.

In this paper, we study the effects of gate length L_g, gate dielectric constant ϵ_{ox}, gate oxide thickness t_{ox}, and source/drain doping concentration on inverse subthreshold slope and on/off current ratio. The gate length and the dielectric constant and thickness have significant effects on on/off current ratio and subthreshold slope. The key quantity is the short channel effects that becomes severe for shorter gate length devices. Relatively longer gate significantly suppresses the tunneling current through the conduction band and improves the subthreshold characteristics. High-K dielectric and thinner oxide also have better gate control that improves the on/off current ratio and subthreshold slope. Improvement of subthreshold slope and drain induced barrier lowering has been observed by shin [8], [9].

II. Simulation Model

The simulation model uses a self-consistent solution between three dimensional (3D) Poisson's equation and effective mass Schrodinger's equation. The 3D Poisson's equation in cartesian coordinates is

$$\frac{\partial}{\partial x}\left(\epsilon\frac{\partial V}{\partial x}\right)+\frac{\partial}{\partial y}\left(\epsilon\frac{\partial V}{\partial y}\right)+\frac{\partial}{\partial z}\left(\epsilon\frac{\partial V}{\partial z}\right)=-\frac{\rho}{\epsilon_o}, \quad (1)$$

where ϵ_o is the free space permittivity, ϵ is the relative dielectric constant, V is the 3D potential, and ρ is the charge density, which is non-zero in silicon nanowire only. Poisson kernel is created by discretizing Eq. (1) using finite difference. Potential is fixed at the gate metal and zero field boundary condition is applied at the source and drain ends and at the exposed surfaces of dielectric. There the normal component of electric field is set to zero. Standard Newton Rapshon method is used to solve Poisson's equation.

The Schrodinger's equation in 3D cartesian coordinates is

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial x}\left(\frac{1}{m_x}\frac{\partial\psi}{\partial x}\right)-\frac{\hbar^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{m_y}\frac{\partial\psi}{\partial y}\right) -\frac{\hbar^2}{2}\frac{\partial}{\partial z}\left(\frac{1}{m_z}\frac{\partial\psi}{\partial z}\right)=E\psi \quad (2)$$

where ψ is the wave function, m_x, m_y, and m_z are the effective masses in device coordinates, and $\hbar$ is the reduced Plank's constant. The nanowire is grown in $\langle 100\rangle$ direction, which is device x coordinate in our study. Ballistic transport is assumed. Recursive Green's function algorithm (RGFA) [10] is used to solve Schrodinger's equation for charge density and current calculations. The open boundary condition in transport direction (x) is included in Schrodinger's equation via self-energy matrices. Hard-wall boundary condition is used in the transverse directions (y and z). For RGFA, the layer (cross-section) Hamiltonian and layer-to-layer coupling matrices are created by discretizing Eq. (2) using finite difference. The charge density at each grid point of the Lth layer (cross-

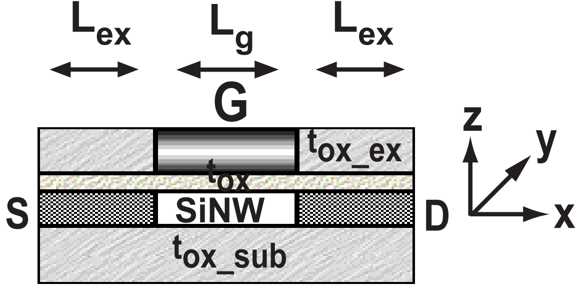

Fig. 1. Device cross section used for simulation. The device coordinates are also shown.

section) is calculated from

$$\rho_i = (4e) \int \frac{dE}{2\pi} \text{diag} \left\{ f_S A^L_{i,i} + f_D \left[A_{i,i} - A^L_{i,i} \right] \right\}, \qquad (3)$$

where e is the electronic charge, f_S and f_D are the source and drain Fermi functions, respectively, and the factor 4 includes spin plus valley degeneracy. The charge density is calculated for each pair of valley and summed over the pairs to obtain the total charge density. The full spectral function is calculated from the imaginary part of retarded Green's function $A_{i,i} = -2\text{Im}\left(G_{i,i}\right)$, where $G = (E - H - \Sigma)^{-1}$. The left spectral function is calculated from $A^L_{i,i} = G_{i,1}\Gamma_{1,1}G^\dagger_{i,1}$, where $\Gamma_{1,1} = i\left(\Sigma_S - \Sigma^\dagger_S\right)$ is the broadening function and the self-energy is calculated from $\Sigma_S = t_{1,0}g_{0,0}t_{0,1}$. Here $t_{0,1}$ is the coupling matrix between the 0th and 1st layers (cross-sections) and $g_{0,0}$ is the surface Green's function calculated using decimation method [11].

The self-consistent loop starts with an initial guess of the potential profile. Anderson mixing [12] scheme is used to accelerate convergence. Once the convergence is achieved, the coherent drain current is calculated from

$$I_D = \frac{2e}{h} \int dE\; T(E) \left(f_S - f_D\right), \qquad (4)$$

where transmission $T(E)$ is calculated from [10]

$$T(E) = \text{tr}\left(\Gamma_{1,1}\left[A_{1,1} - G_{1,1}\Gamma_{1,1}G^\dagger_{1,1}\right]\right). \qquad (5)$$

III. Simulation Results

The top gate silicon nanowire on insulator device used in our simulation is shown in Fig. 1. The silicon nanowire is placed on a thick substrate oxide layer t_{ox-sub}. The gate oxide of thickness t_{ox} is grown on the nanowire. An ultra-thin gate metal is deposited on the top of the gate oxide and the exposed regions on both sides of the gate metal are covered by oxide t_{ox-ex}. The nanowire has a square cross section of 5×5 nm^2 with a band gap E_g of 1.38 eV. The doped source-drain extension L_{ex} is 20 nm and fully ionized uniform donor concentration is assumed. The channel is undoped. The substrate oxide and the extended oxide are assumed to be SiO_2 with a dielectric constant of 3.9. The gate metal is assumed to have the same work function value as the nanowire has. The t_{ox-sub} value of 5 nm and the t_{ox-ex} value of 5 nm are considered for Poisson solver so that the fringing electric fields emanating from the gate metals are treated correctly. The nanowire is modeled using bulk effective mass whose accuracy for wire cross section of 5×5 nm^2 and above has been varified [13], [14].

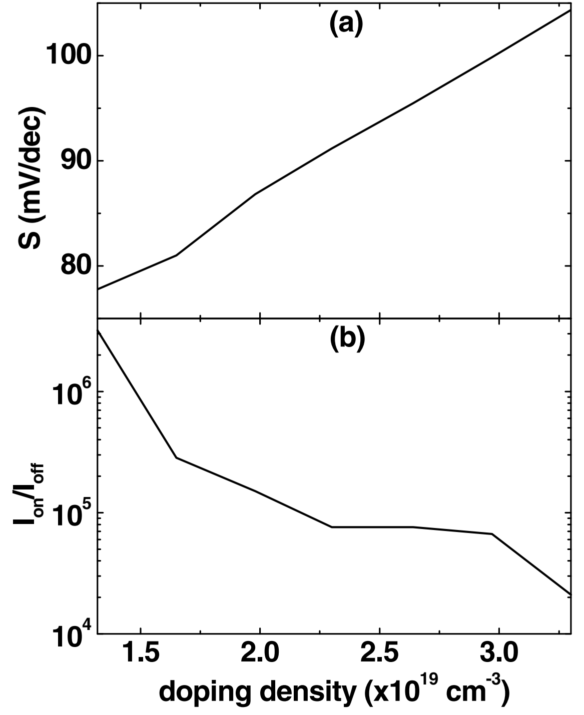

Fig. 2. Inverse subthreshold slope and on/off current ratio versus doping concentration.

The simulated inverse subthreshold slope S and the on/off current ratio versus doping concentration are shown in Fig. 2. The simulation is performed for devices with gate length L_g of 10 nm, gate oxide thickness t_{ox} of 1 nm, and gate dielectric constant ϵ_{ox} of 3.9. The on/off current ratio reduces and the inverse subthreshold slope increases with higher doping concentration. If we double the doping concentration, the on/off current ratio is reduced by more than one order of magnitude and the inverse subthreshold slope becomes about 1.3 times. The scaling behavior of inverse subthreshold slope and on/off current ratio with gate length L_g is shown in Fig. 3. The devices used for simulation have gate oxide thickness t_{ox} of 1 nm, gate dielectric constant ϵ_{ox} of 3.9 and doping concentration of 1.65 $\times 10^{19}$ cm^{-3}. Device performance degrades with shorter gate due to short channel effects. The key quantity is the tunneling current through the conduction band that increases significantly for shorter gate devices. With longer gate length, the off current improves significantly and the on current degrades slightly that results in significant improvement in on/off current ratio. For example, the off current (mainly tunneling current) improves from .047 μA to 1.23 $\times 10^{-5}\mu$A and the on current degrades from 25.2 μA to 11.3 μA when the gate length changes from 5 nm to 10 nm. This change in gate length improves the on/off current ratio by

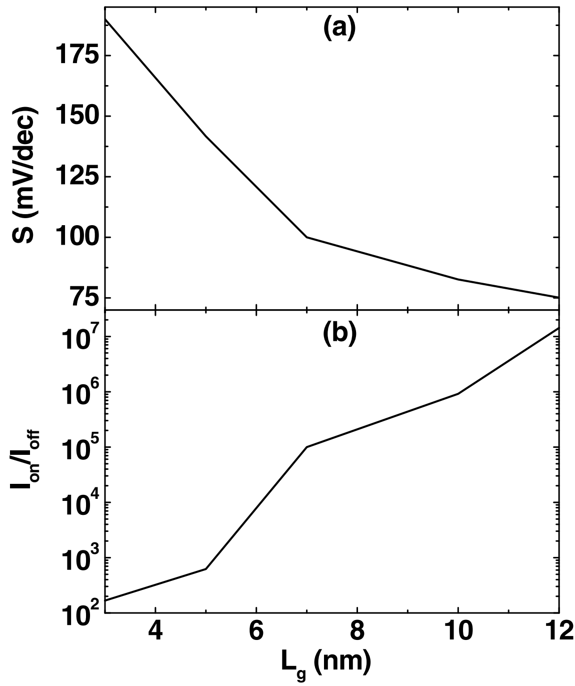

Fig. 3. Inverse subthreshold slope and on/off current ratio versus gate length.

three orders of magnitude and the inverse subthreshold slope from 141.68 mV/dec to 82.59 mV/dec.

Next we study the effects of gate dielectric constant and thickness on the inverse subthreshold slope and on/off current ratio. Simulation results of inverse subthreshold slope and on/off current ratio as a function of gate dielectric constant ϵ_{ox} are shown in Fig. 4. Both the inverse subthreshold slope and the on/off current ratio improve with high-K gate dielectric. The change of gate dielectric constant from 3.9 to 14 improves the on/off current ratio by two orders of magnitude and the inverse subthreshold slope from 81 mV/dec to 70 mV/dec. The physics can be understood from the band diagram shown in Fig. 5 for two different gate dielectric constant 3.9 and 14. Note that only the conduction bands are shown because the tunneling current through the valence band is zero. From the band profiles we see that the gate control is much better with high-K gate dielectric in off state. The channel potential barrier is almost equal to $E_g/2e$ that reduces the tunneling plus thermal current significantly. On the other hand, the modulation of band profile in on state with gate dielectric constant is insignificant, and therefore, the change in on current with ϵ_{ox} is very little. The off current improves from $1.23 \times 10^{-5} \mu$A to $5.65 \times 10^{-8} \mu$A and the on current degrades from 11.3 μA to 9.0 μA when the ϵ_{ox} changes from 3.9 to 14.

The scaling of inverse subthreshold slope and on/off current ratio with t_{ox} is shown in Fig. 6. The devices used for simulation have gate length L_g of 10 nm, gate dielectric constant ϵ_{ox} of 3.9, and doping concentration of 1.65×10^{19} cm^{-3}. Both the inverse subthreshold slope and the on/off

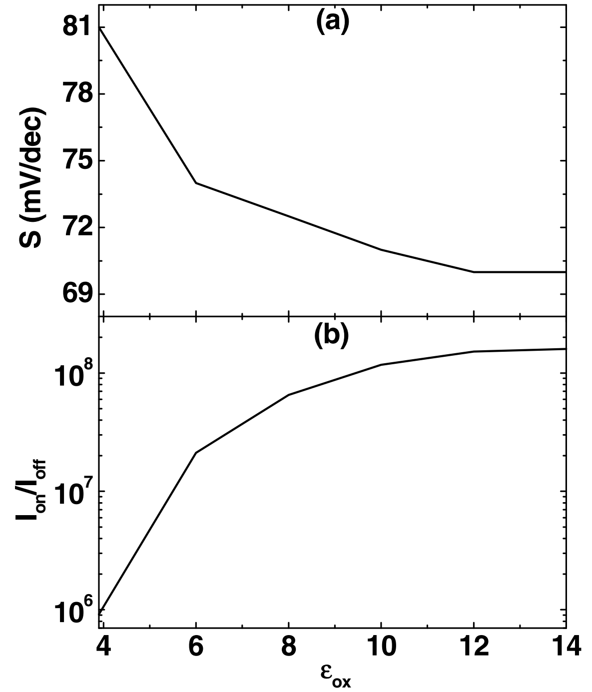

Fig. 4. Inverse subthreshold slope and on/off current ratio versus gate dielectric constant ϵ_{ox}.

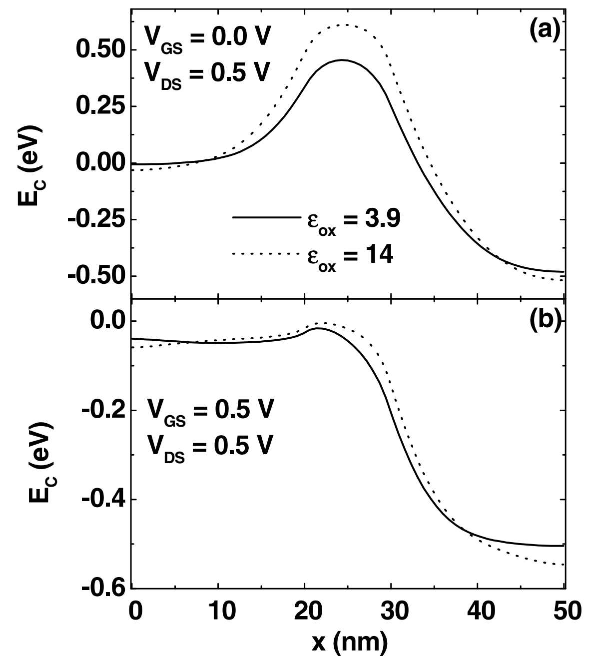

Fig. 5. Conduction band profile for two dielectric constant in (a) off state (b) on state.

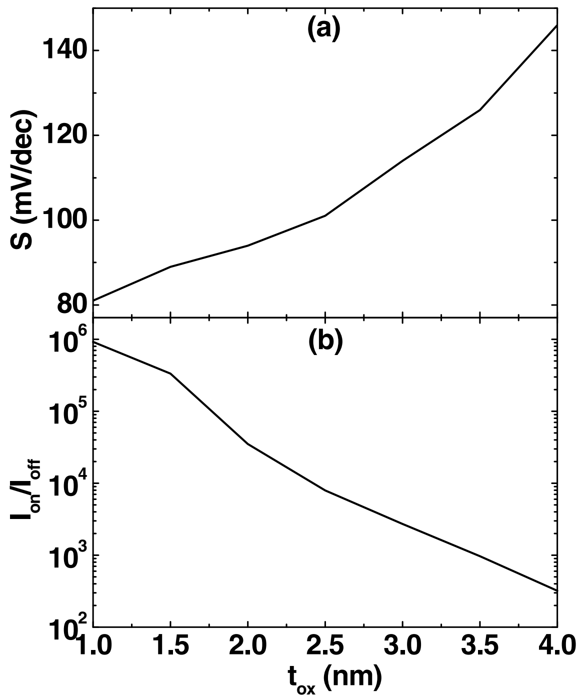

Fig. 6. Inverse subthreshold slope and on/off current ratio versus gate dielectric thickness t_{ox}.

current ratio significantly improve with thinner oxide due to better gate control with thin gate oxide. For a change of t_{ox} from 4 nm to 1 nm, the on/off current ratio improves more than three orders of magnitude and the inverse subthreshold slope improves from 146 to 81.

IV. Conclusion

A three dimensional quantum simulation is performed to study the effects of doping, gate length, gate dielectric constant, and thickness on inverse subthreshold slope and on/off current ratio of a top gate silicon nanowire on insulator transistor. The device performance in terms of inverse subthreshold slope and on/off current ratio improves with thinner high-K gate dielectric and relatively longer gate length.

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